In the Claims:

Claims 1-29 (canceled)

Claim 30 (previously presented): A flip-chip semiconductor device comprising:

a semiconductor die having a first major surface and a second major surface opposite from and substantially parallel to said first major surface, said semiconductor die including a highly doped substrate of a first conductivity type, a P/N junction receiving layer of said first conductivity type formed over said highly doped substrate, and at least one diffusion region of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region of said first conductivity type formed in said diffusion region, said highly doped region in contact with a first power electrode formed over said first major surface;

a high conductivity region connecting said highly doped substrate with a second power electrode formed over said first major surface and laterally spaced apart from said first power electrode;

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component oriented substantially perpendicular to said first major surface.

Claim 31 (previously presented): The flip-chip semiconductor device of claim 30, further comprising a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 μm.

Claim 32 (previously presented): The flip-chip semiconductor device of claim 30, further comprising a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode, wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm.

Claims 33-34 (canceled)

Claim 35 (previously presented): The flip-chip semiconductor device of claim 30, wherein said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type.

Claim 36 (previously presented): The flip-chip semiconductor device of claim 30, wherein said high conductivity region connecting said highly doped substrate with said second power electrode comprises a metallic material residing in a trench formed in

said semiconductor die and extending from said first major surface towards said second major surface.

Claim 37 (canceled)

Claim 38 (previously presented): The flip-chip semiconductor device of claim 30, further comprising a control electrode formed over said first major surface.

Claims 39-40 (canceled)

Claim 41 (previously presented): A flip-chip semiconductor device comprising:

a semiconductor die having a first major surface and a second major surface opposite from and substantially parallel to said first major surface, said semiconductor die including a highly doped substrate of a first conductivity type, a P/N junction receiving layer of said first conductivity type formed over said highly doped substrate, and at least one diffusion region of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped source region of said first conductivity type formed in said diffusion region adjoining an insulated gate structure of said flip-chip semiconductor device, said highly doped source region in contact with a source electrode formed over said first major surface;

a high conductivity region connecting said highly doped substrate with a drain electrode formed over said first major surface and laterally spaced apart from said source electrode;

wherein a conductive path from said source electrode to said drain electrode includes at least one vertical component oriented substantially perpendicular to said first major surface.

Claim 42 (previously presented): The flip-chip semiconductor device of claim 41, further comprising a first solder ball formed on said source electrode and a second solder ball formed on said drain electrode, wherein said first and second solder balls have a width of greater than or equal to approximately 200 μm.

Claim 43 (previously presented): The flip-chip semiconductor device of claim 41, further comprising a first solder ball formed on said source electrode and a second solder ball formed on said drain electrode, wherein said first and second solder balls are separated by a pitch of greater than or equal to approximately 0.8 mm.

Claims 44-45 (canceled)

Claim 46 (previously presented): The flip-chip semiconductor device of claim 41, further comprising a gate electrode formed over said first major surface and laterally spaced from said source electrode and said drain electrode.

Claim 47 (previously presented): The flip-chip semiconductor device of claim 41, wherein said insulated gate structure is situated entirely over said first major surface.

Claim 48 (previously presented): The flip-chip semiconductor device of claim 41, wherein said insulated gate structure comprises:

an insulated trench formed in said semiconductor die, said insulated trench extending from said first major surface towards said highly doped substrate; and

a polysilicon gate residing entirely within said insulated trench.

Claim 49 (previously presented): The flip-chip semiconductor device of claim 41, wherein said high conductivity region connecting said highly doped substrate with said drain electrode is one of a highly doped sinker region of said first conductivity type, and a metallic material residing in a trench formed in said semiconductor die and extending from said first major surface towards said second major surface.

Claim 50 (new): A flip-chip semiconductor device comprising:

a semiconductor die including a highly doped substrate of a first conductivity type, a P/N junction receiving layer of said first conductivity type formed over said highly doped substrate, and at least one diffusion region of a second conductivity type forming at least one respective P/N junction at an interface with said P/N junction receiving layer;

a highly doped region of said first conductivity type, said highly doped region in contact with a first power electrode;

a high conductivity region connecting said highly doped substrate with a second power electrode formed;

wherein a conductive path from said first power electrode to said second power electrode includes at least one vertical component in said semiconductor die.

Claim 51 (new): The flip-chip semiconductor device of claim 50, further comprising a first solder ball formed on said first power electrode and a second solder ball formed on said second power electrode.

Claim 52 (new): The flip-chip semiconductor device of claim 50, further comprising a first plurality of contact bumps formed on said first power electrode and a second plurality of contact bumps formed on said second power electrode.

Claim 53 (new): The flip-chip semiconductor device of claim 50, wherein said high conductivity region connecting said highly doped substrate with said second power electrode comprises a highly doped sinker region of said first conductivity type.

Claim 54 (new): The flip-chip semiconductor device of claim 50, wherein said high conductivity region connecting said highly doped substrate with said second power electrode comprises a metallic material residing in a trench formed in said semiconductor die.